REMARKS

Reconsideration of the above-identified application in view of the preceding amendments and following remarks is respectfully requested. Claims 1-10, 20 and 21 are pending in this application. By this Amendment, Applicants have amended Claims 1, 20 and 21. The claim amendments were made to more precisely define the invention in accordance with 35 U.S.C. 112, paragraph 2. These amendments have not been necessitated by the need to distinguish the present invention from any prior art. It is respectfully submitted that no new matter has been introduced by these amendments, as support therefor is found throughout the specification and drawings.

In the Office Action, Claims 1-4, 7, 8, 20 and 21 were rejected under 35 U.S.C. §102(b) over Japanese patent application no. 2001-351995 to Shigenobu et al. The Examiner's grounds for rejection are herewith traversed, and reconsideration is respectfully requested.

Shigenobu et al. disclose a semiconductor with a high-voltage circuit section separated by the isolation insulator layer 45 with the memory cell array section. A low-battery section is separated by the isolation insulator layer 45 with memory cell array section is shown in Figure 36 and described in paragraphs 104-106. Memory cell transistors are divided by an isolation insulators layer 5. The high-voltage transistors, which adjoin mutually, are separated by the isolation insulator layer 5. In other words and as clearly shown in Figure 36, the memory cell has transistors with wells 47 on one side and different wells 5 on the other.

In contrast, Claim 1 recites a semiconductor device including a support substrate, an insulating layer formed on the support substrate, a first semiconductor layer formed on the insulating layer, a first high breakdown voltage transistor formed in

the first semiconductor layer, a second semiconductor layer formed on the insulating layer, a second high breakdown voltage transistor formed in the second semiconductor layer, a first isolation region formed between the first semiconductor layer and the second semiconductor layer, the first isolation region surrounding the first and second high breakdown voltage transistors and having a depth that reaches the insulating layer, a third semiconductor layer formed on the insulating layer, a first low breakdown voltage transistor formed in the third semiconductor layer, a second low breakdown voltage transistor formed in the third semiconductor layer, and a second isolation region formed in the third semiconductor layer between the first low breakdown voltage transistor and the second first low breakdown voltage transistor, the second isolation region having a depth that does not reach the insulating layer. Consequently, no matter which side of the high-voltage transistors you look at, you will find the first isolation region with a depth that goes to the insulating layer as shown in Figure 1. As a result, the formation of a parasitic MOS transistor is inhibited and the area of the high breakdown voltage transistor can be reduced (see page 9, 3rd paragraph of the subject application). Shigenobu et al. do not disclose or suggest such a structural configuration because on at least one side, it does not reach the insulating layer. Accordingly, Claim 1 and each of the remaining claims depending therefrom distinguish the subject invention from Shigenobu et al. and an action acknowledging the same is respectfully requested.

With respect to Claim 20, Shigenobu et al. only show memory cells having transistors with wells 47 that go down to the insulating layer on one side as noted above. However, Claims 20 recites a semiconductor device including a support substrate, an insulating layer formed on the support substrate, a high breakdown

voltage transistor, a low breakdown voltage transistor, wherein the high breakdown voltage transistor is within a first isolation region having a depth that reaches the insulating layer, and the low breakdown voltage transistor is adjacent to a second isolation region having a depth that does not reach the insulating layer. Shigenobu et al. do not disclose or suggest such a structural configuration. Thus, Claim 20 distinguishes the subject invention from Shigenobu et al. and an action acknowledging the same is respectfully requested.

With respect to Claim 21, Shigenobu et al. disclose wells 5 that are formed at the same time as wells 47 but no other structure is formed at the same time. In contrast, Claim 21 recites a method of manufacturing a semiconductor device including the steps of preparing a substrate including a support substrate and an insulating layer, forming a first isolation region having a depth that reaches the insulating layer, wherein the first isolation region includes a first trench insulating layer, forming a second isolation region having a depth that does not reach the insulating layer, wherein the second isolation region includes a second trench insulating layer, forming a first high breakdown voltage transistor in a region within the first isolation region, wherein the first high breakdown voltage transistor includes a trench insulating offset, and forming a first low breakdown voltage transistor in a region adjacent to the second isolation region, wherein the first trench insulating layer, the second trench insulating layer and the trench insulating offset are all formed simultaneously. For an exemplary embodiment of this, the Examiner's attention is directed to Figures 7-9 and the associated description on pages 11 and 12 of the subject application. As a result of this claimed method, the number of process steps is advantageously reduced. Shigenobu et al. do not disclose or suggest such a process. Further, similarly to as

noted above, the first high voltage breakdown transistor is within the first isolation region and Shigenobu et al. does not disclose this either. For at least these reasons, Claim 21 distinguishes the subject invention from Shigenobu et al. and an action acknowledging the same is respectfully requested.

In the Office Action, Claims 5 and 6 were rejected under 35 U.S.C. § 103 (a) over Shigenobu et al.

The Examiner took Official Notice that the limitations of the claims were notoriously well known in the prior art. The applicant hereby seasonably traverses such Official Notice and requests evidence in support of it in the event that the rejections are maintained. Additionally, it is respectfully reiterated that the deficiencies of Shigenobu et al. noted above remain and, therefore, Claims 5 and 6 by virtue of their dependency upon Claim 1, patentably distinguish over the art of record and an action acknowledging the same is respectfully requested.

In the Office Action, Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) over Shigenobu et al. in view of U.S. Patent No. 5,965,921 to Kojima.

It is respectfully submitted that Kojima does not overcome the deficiencies of Shigenobu et al., as noted above with respect to Claim 1. In particular, neither Shigenobu et al. nor Kojima disclose or suggest, either alone or in combination, in whole or in part, a semiconductor device including, *inter alia,* the first isolation region surrounding the first and second high breakdown voltage transistors and having a depth that reaches the insulating layer as recited in Claim 1. Accordingly, Claims 9 and 10, by virtue of their dependence on Claim 1, are not rendered obvious by the combination of references cited by the Examiner and withdrawal of the rejection under 35 U.S.C. §103 (a) is respectfully requested.

Any additional fees or overpayments due as a result of filing the present paper may be applied to Deposit Account No. 04-1105. It is respectfully submitted that all of the claims now remaining in this application are in condition for allowance, and such action is earnestly solicited.

If after reviewing this amendment, the Examiner believes that a telephone interview would facilitate the resolution of any remaining matters the undersigned attorney may be contacted at the number set forth herein below.

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Respectfully submitted,

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